

**REMARKS**

**Related to the Claims**

Claims 1, 2, 4, and 17 were amended. Claim 2 was amended to correct an informality; claims 1, 2, and 17 were amended to more clearly claim the disclosed circuit structures (as shown, *e.g.*, as transistors 23 and 33 in Figure 1).

Reconsideration of the claims is respectfully requested.

**Claim Rejections -- 35 U.S.C. § 102**

Claims 1-20 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,177,839 to *Ishihara*.

Independent claims 1, 4, and 17 have been amended to more clearly claim the circuit structures as shown, *e.g.*, as transistors 23 and 33 in Figure 1. These transistors, as described on page 8 (and elsewhere) of the previously-submitted substitute specification, constitute the second sub-branches of the second output branch of the second and third differential amplifier stages, respectively. Connected directly to the current power supply terminal 15 in Figure 1, these transistors, in at least some modes of operation, do not contribute to the signal gain, as described on page 10 of the substitute specification.

This may be contrasted with corresponding transistors 11 and 12 of *Ishihara*'s second and third amplifier stages, which are cross-connected to the output branches of the opposing amplifier stages, and each always contributes to the minimum gain (see, *e.g.*, col 7, lines 21-24).

Nothing in *Ishihara* teaches or suggests the circuit structure as described in the specification and claimed herein.

Therefore, the rejection of claims 1-20 under 35 U.S.C. § 102 has been overcome.

SUMMARY

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at *wmunck@davismunck.com*.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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